

GA-F2A68HM-S1

PAGE TITLE *Revision : 1.0*

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03	BLOCK DIAGRAM
04	APU DDRIII MEMORY
05	APU CONTROL
06	APU UMI, GFX, GPP
07	APU POWER & GND
08	DDRIII CHANNEL A
09	Bolton 68H UMI, PCIE, PCI, CPU, LPC
10	Bolton 68H ACPI, GPIO, USB, AUDIO
11	Bolton 68H SATA,SPI,HWM
12	Bolton 68H POWER & GND
13	PCIE x16 , x1
14	PCI SLOT
15	ITE 8620 (DUAL BIOS CO-LAY), KB/MS , HWMO
16	VGA ,RGB
17	FAN ,USB30,F_USB2
18	ALC887-VD2 CODEC
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20	POWER SEQUENCE
21	VCORE (ISL62773)
22	VCORE MOS
23	DDR POWER, 5VDUAL , ERP
24	RTL8111G
25	VCC_SB , APU_VDDP , VCC11_DUAL , VDDA25

APU_VDDIO_SUS=DDR15V

APU_VTT_SUS=DDRVTT

APU_VDDP_RUN=APU_VDDR_RUN=APU_VDDP

+1.1V_RUN=FCH_VDD_11_RUN=VCC_SB


+3.3V_RUN=VCC3

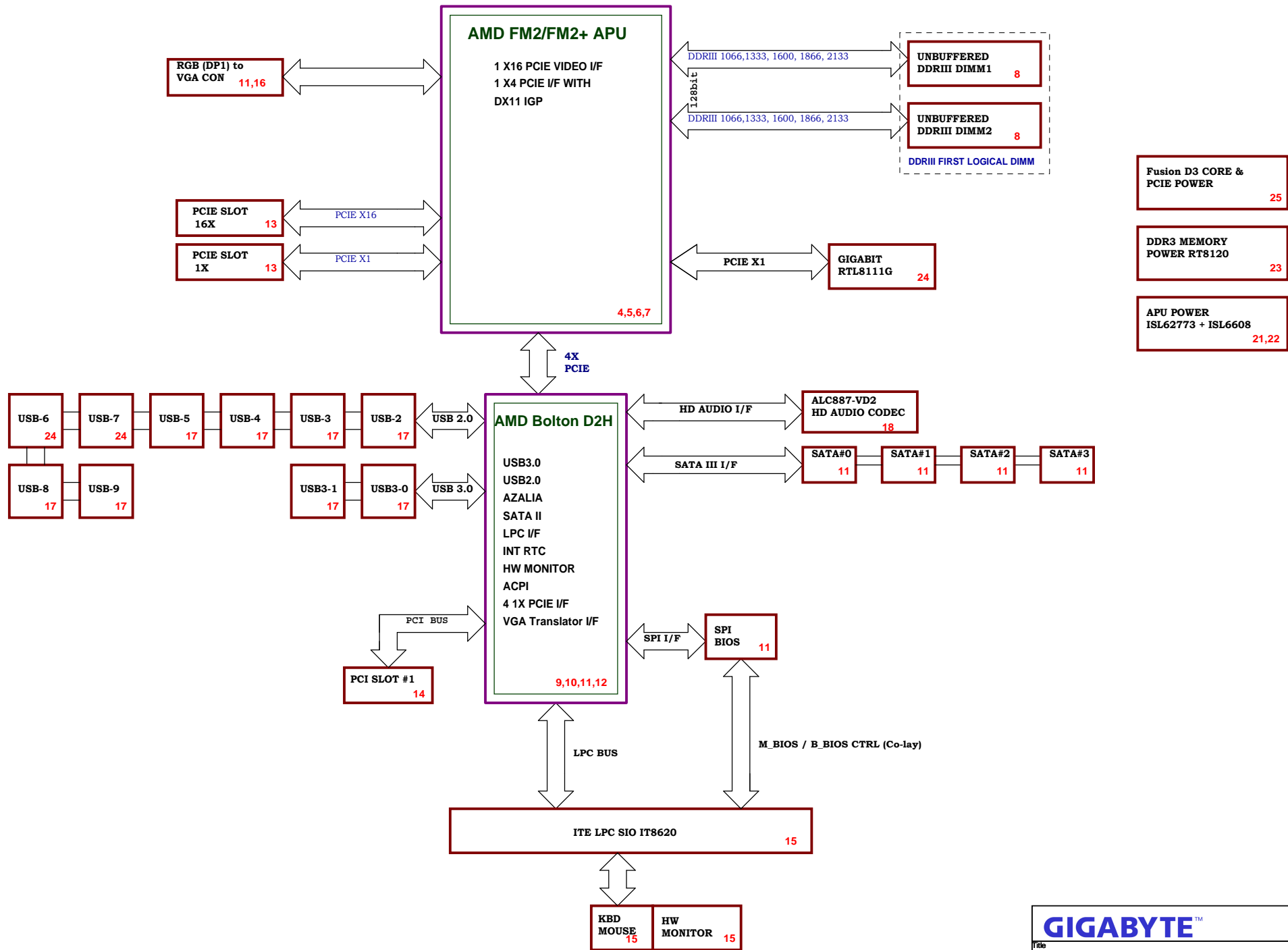
+3.3V_ALW=3VDUAL

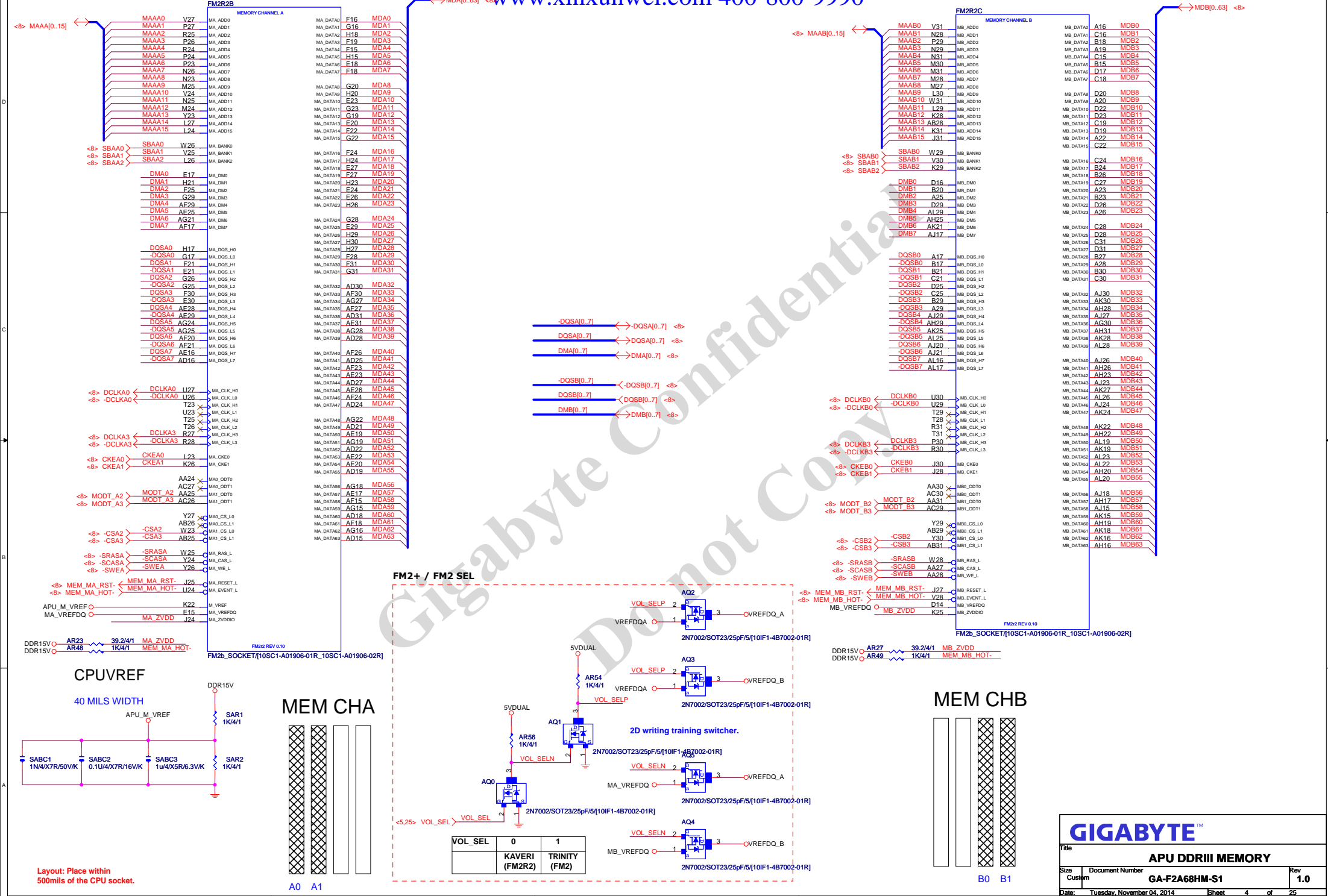
GIGABYTE™			
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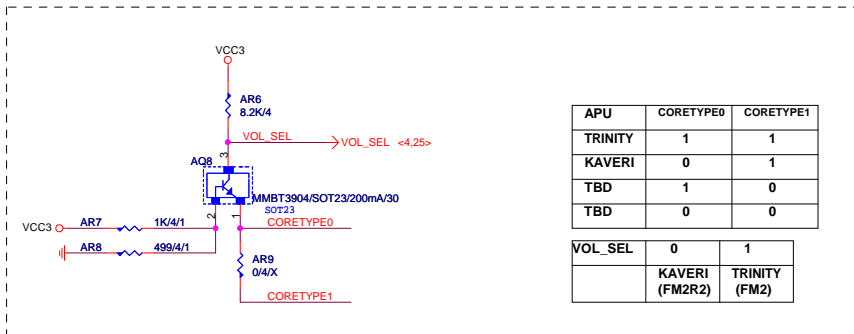
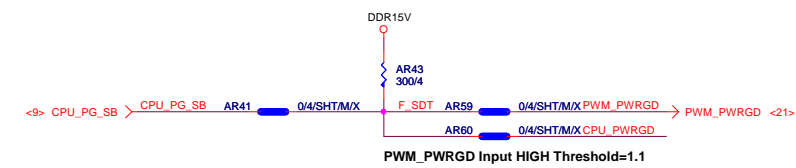
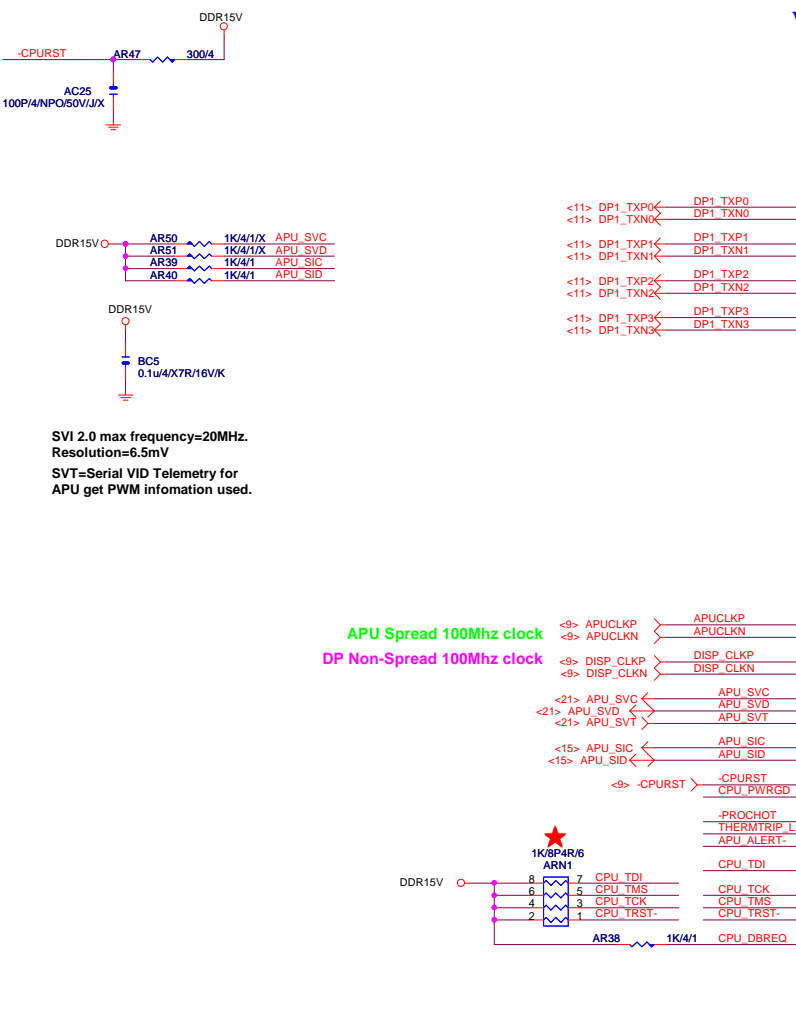
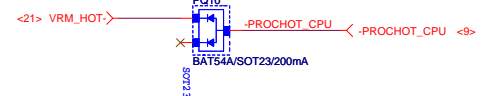
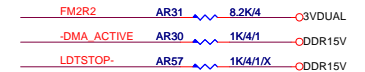
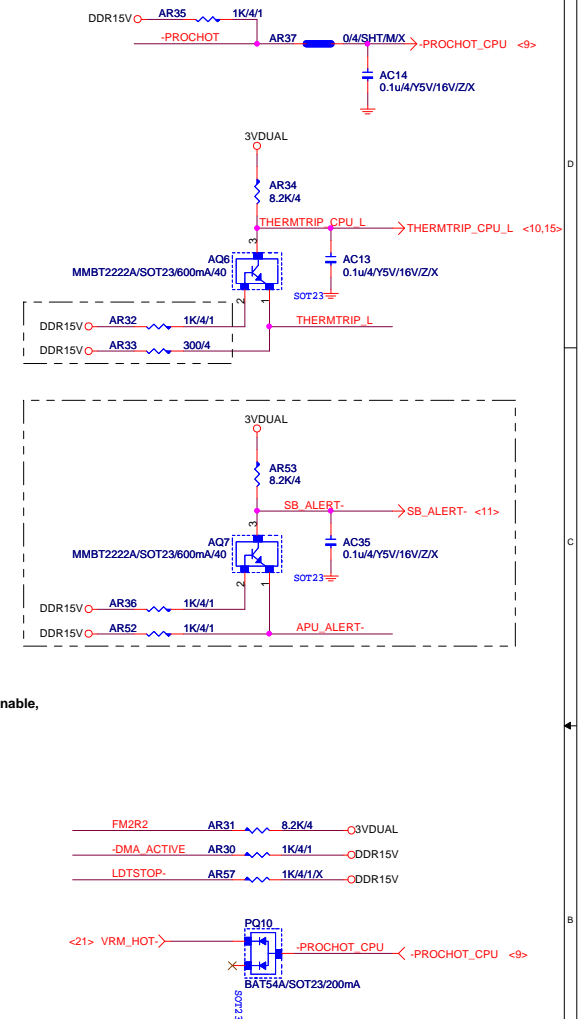
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Title				
BOM & PCB HISTORY				
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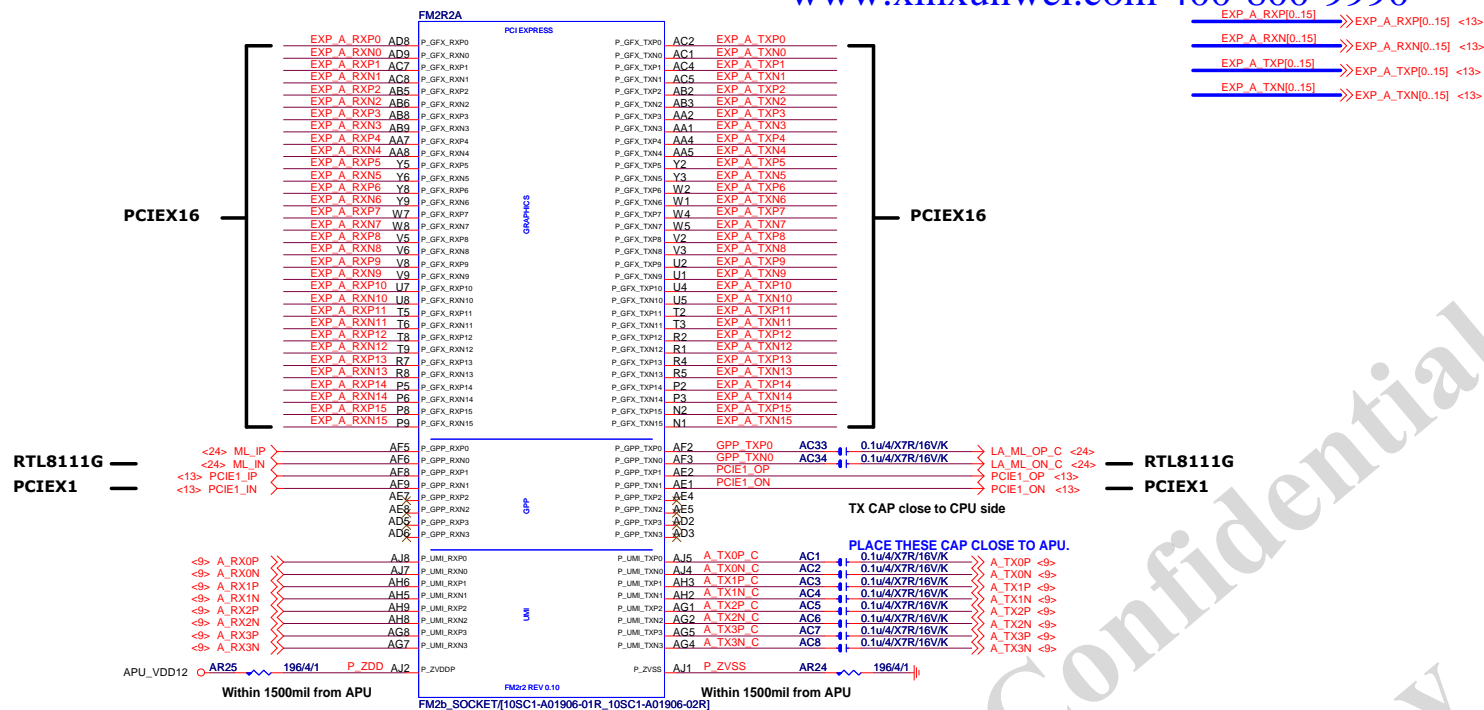


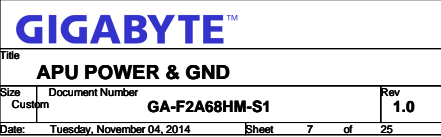


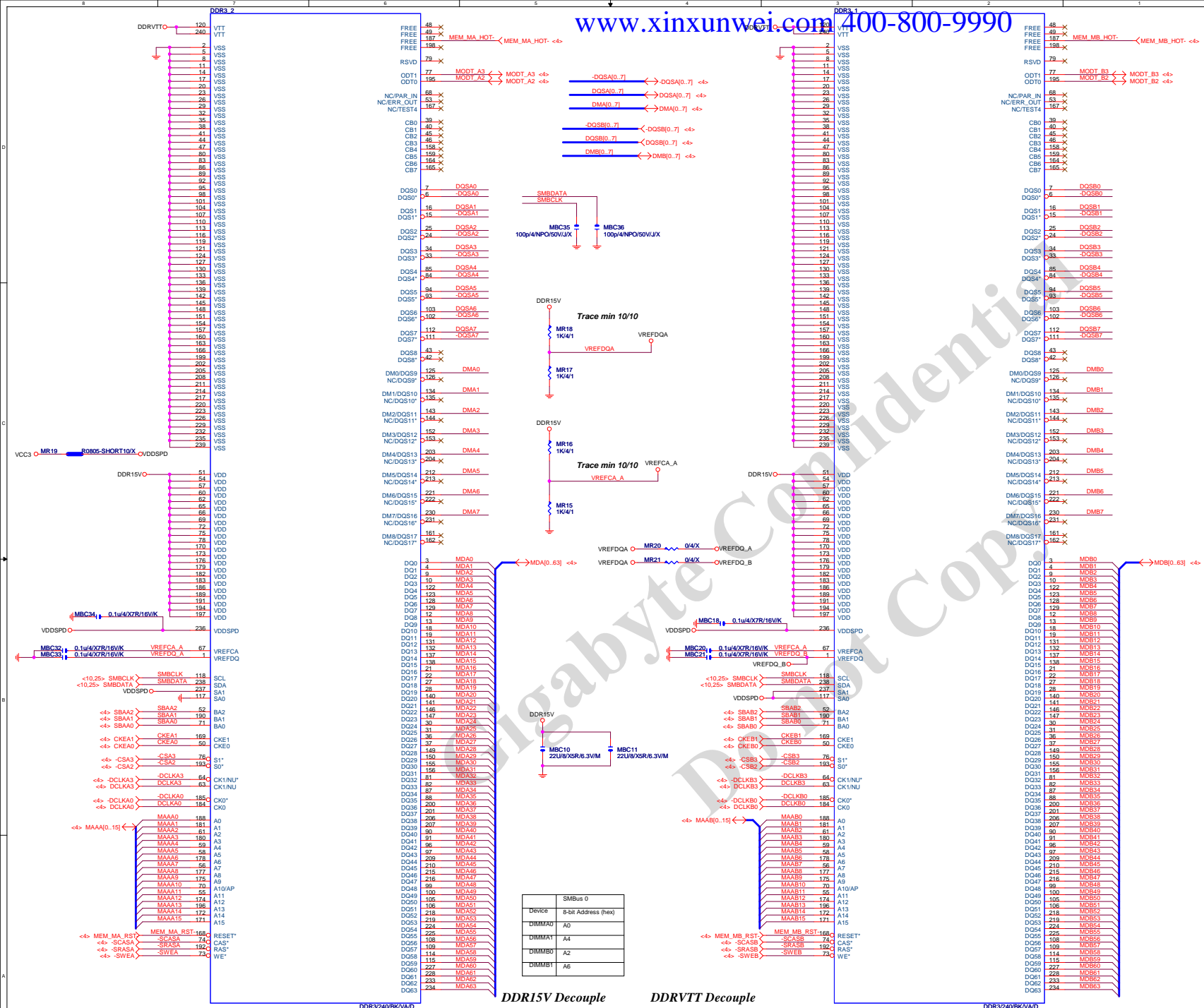


APU	CORETYPE0	CORETYPE1
TRINITY	1	1
KAVERI	0	1
TBD	1	0
TBD	0	0

VOL_SEL	0	1
	KAVERI (FM2R2)	TRINITY (FM2)



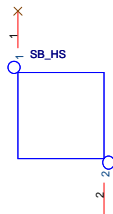




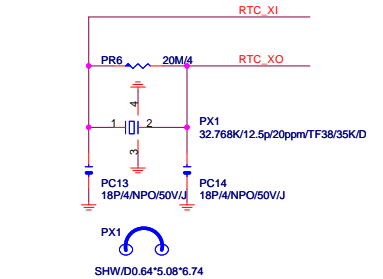


PLACE THESE PCIE AC COUPLING
CAPS CLOSE TO SB850

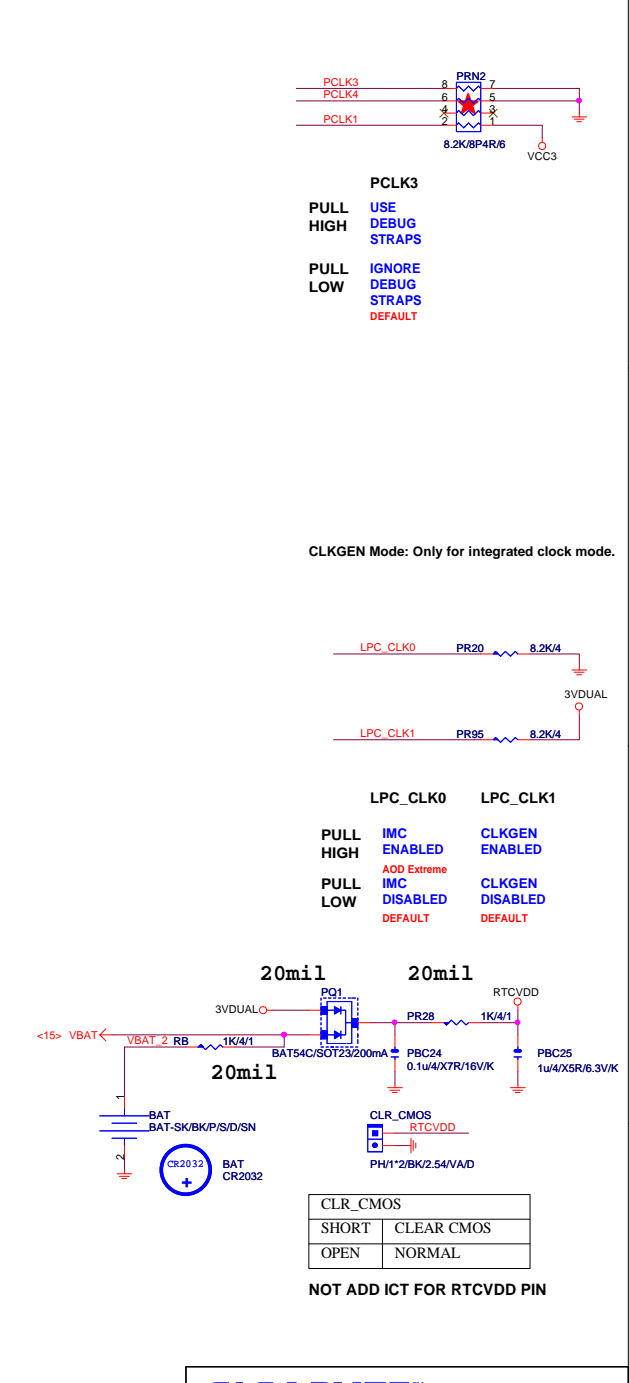
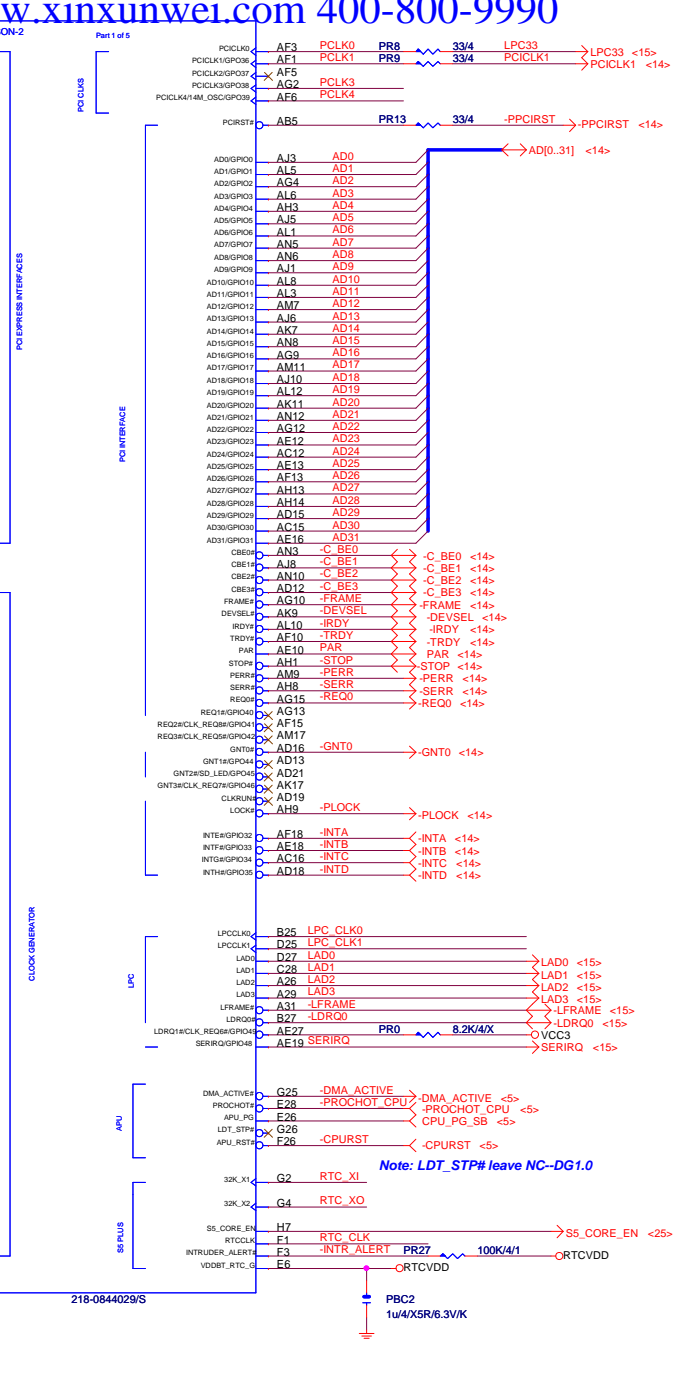
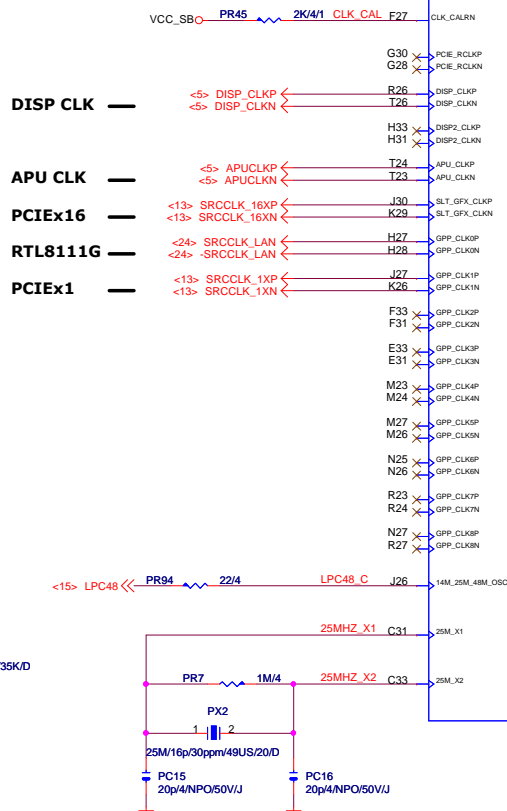
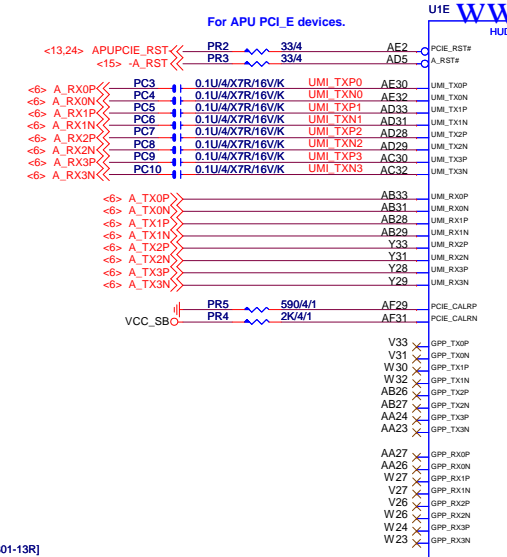
S.B HEATSINK



SB_HS[12SP2-SA0301-11R_12SP2-SA0301-12R_12SP2-SA0301-13R]



SHW/D0.64*5.08*6.74

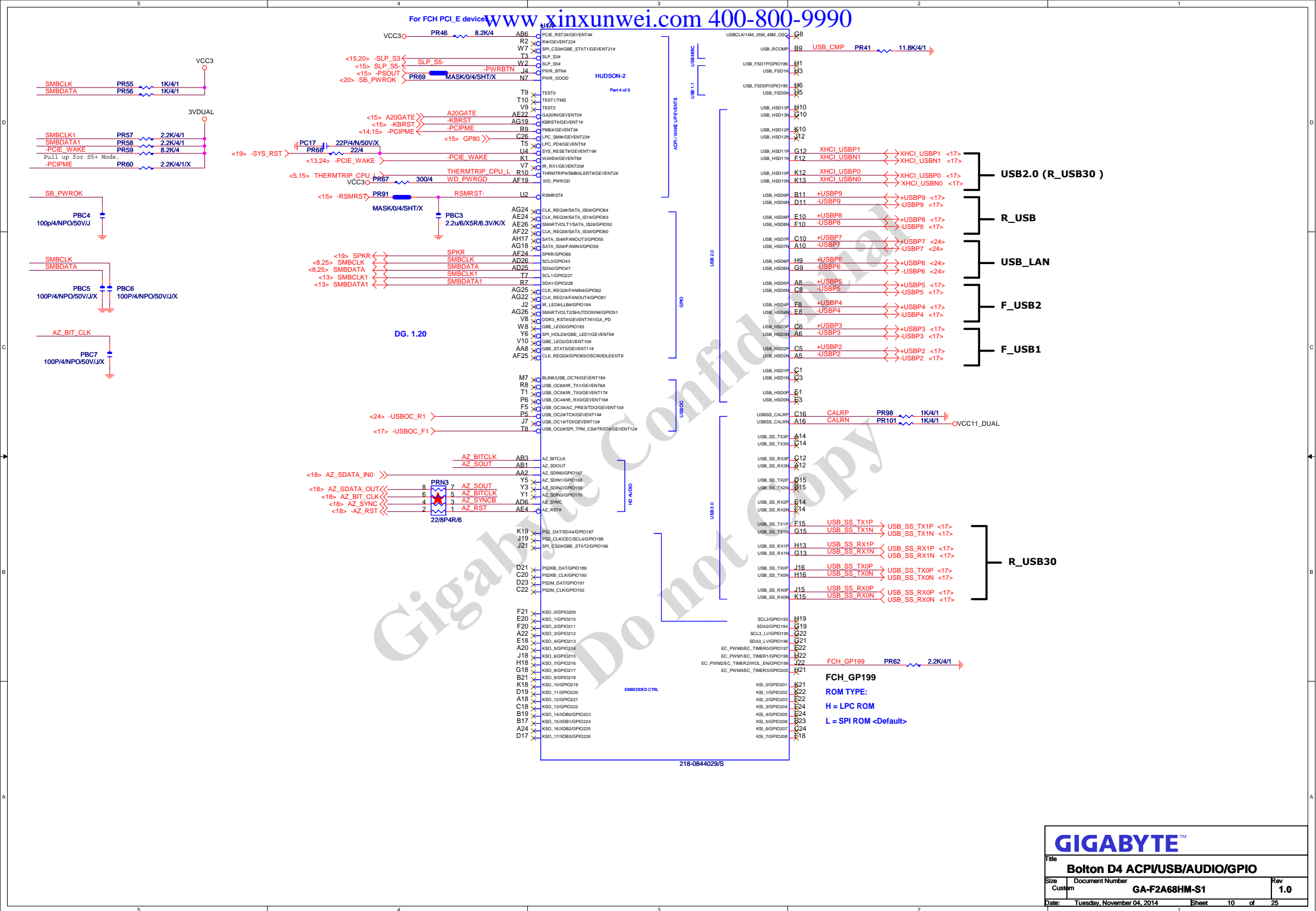


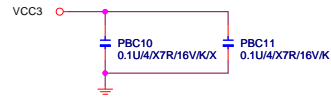
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Bolton D4PCIE/PCI/CPU/LPC

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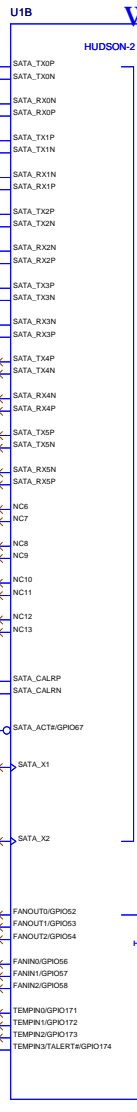
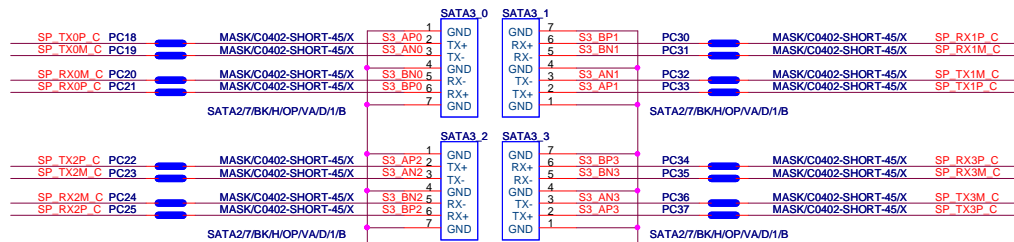
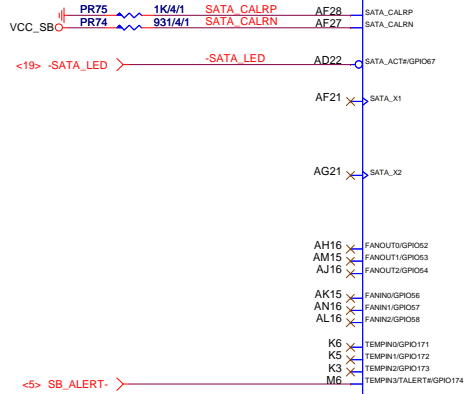
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SATA 6~7 for Hudson D4.

PLACE SATA_CAL RES VERY CLOSE TO BALL OF U1



Part 2 of 5

SD_CLK#CLK_2/GPIO73 AL14

SD_CMD#CMD_2/GPIO74 AN14

SD_CD#GPIOW75 AJ12

SD_WP#GPIOW76 AH12

SD_DATA0SDAT1_2/GPIO77 AK13

SD_DATA1SDAT2_2/GPIO78 AM13

SD_DATA2GPIOW79 AH15

SD_DATA3GPIOW80 AJ14

RGMII NOT SUPPORT. DG:1.20

GBE_COL AC4

GBE_CRS AD3

GBE_MDCK AD9

GBE_MDIO W10

GBE_RXCLK AB8

GBE_RXD0 AH7

GBE_RXD2 AF7

GBE_RXD1 AE7

GBE_RXD0 AD7

GBE_RXCTLRXDV AG8

GBE_RXENH AD1

GBE_TXCLK AB7

GBE_TXD3 AF9

GBE_TXD2 AG6

GBE_TXD1 AE9

GBE_TXD0 AD8

GBE_TXCTLTXEN AB9

GBE_PHY_PD AC2

GBE_PHY_RSTB AA7

GBE_PHY_INTB W9

V5 SB SPI DI_R

V5 SB SPI DO_R

V3 SB SPI CLK_R

T6 SB SPI CS_

V1 SB SPI WP_ TP1

VGA_RED L30

VGA_GREEN L32

VGA_BLUE M29

M28 DAC_HSYNC

N30 DAC_VSYNC

M33 DDCDATA

N32 DDCCLK

VGA_DDC_SDVAGPIOW75 K31

AUX_VGA_CH_F V28

AUX_VGA_CH_N V29

AUXCAL U28

T31 SW VGA TXD0+ HC19

T33 SW VGA TXD0- HC20

T29 SW VGA TXD1+ HC15

T28 SW VGA TXD1- HC16

R32 SW VGA TXD2+ HC17

R30 SW VGA TXD2- HC18

P29 SW VGA TXD3+ HC21

P28 SW VGA TXD3- HC22

ML_VGA_L1P ML_VGA_L0N

ML_VGA_L1P ML_VGA_L1N

ML_VGA_L2P ML_VGA_L2N

ML_VGA_L3P ML_VGA_L3N

ML_VGA_HPDPGPIOW229 C29

VIN0GPIOW175 N2

VIN1GPIOW176 M3

VIN2SDAT1_1GPIOW177 L2

VIN3SDAT0_1GPIOW178 N4

VIN4SLOAD_1GPIOW179 P1

VIN5SCLK_1GPIOW180 P3

VIN6GBE_STAT3GPIOW181 M1

VIN7GBE_LED3GPIOW182 M5

K6 TEMPIN1GPIOW171

K5 TEMPIN1GPIOW172

K3 TEMPIN2GPIOW173

M6 TEMPIN3TALERT3GPIOW174

PC30 MASK/C0402-SHORT-45/X

PC31 MASK/C0402-SHORT-45/X

PC32 MASK/C0402-SHORT-45/X

PC33 MASK/C0402-SHORT-45/X

PC34 MASK/C0402-SHORT-45/X

PC35 MASK/C0402-SHORT-45/X

PC36 MASK/C0402-SHORT-45/X

PC37 MASK/C0402-SHORT-45/X

PC38 MASK/C0402-SHORT-45/X

PC39 MASK/C0402-SHORT-45/X

PC40 MASK/C0402-SHORT-45/X

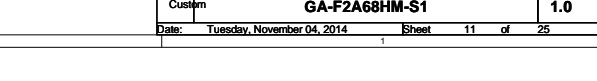
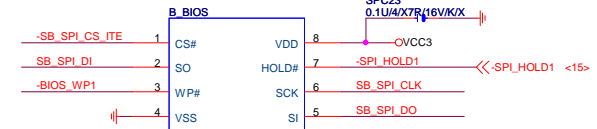
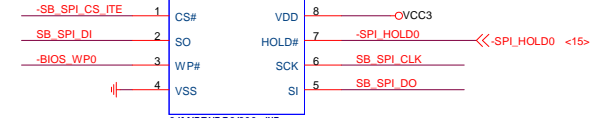
PC41 MASK/C0402-SHORT-45/X

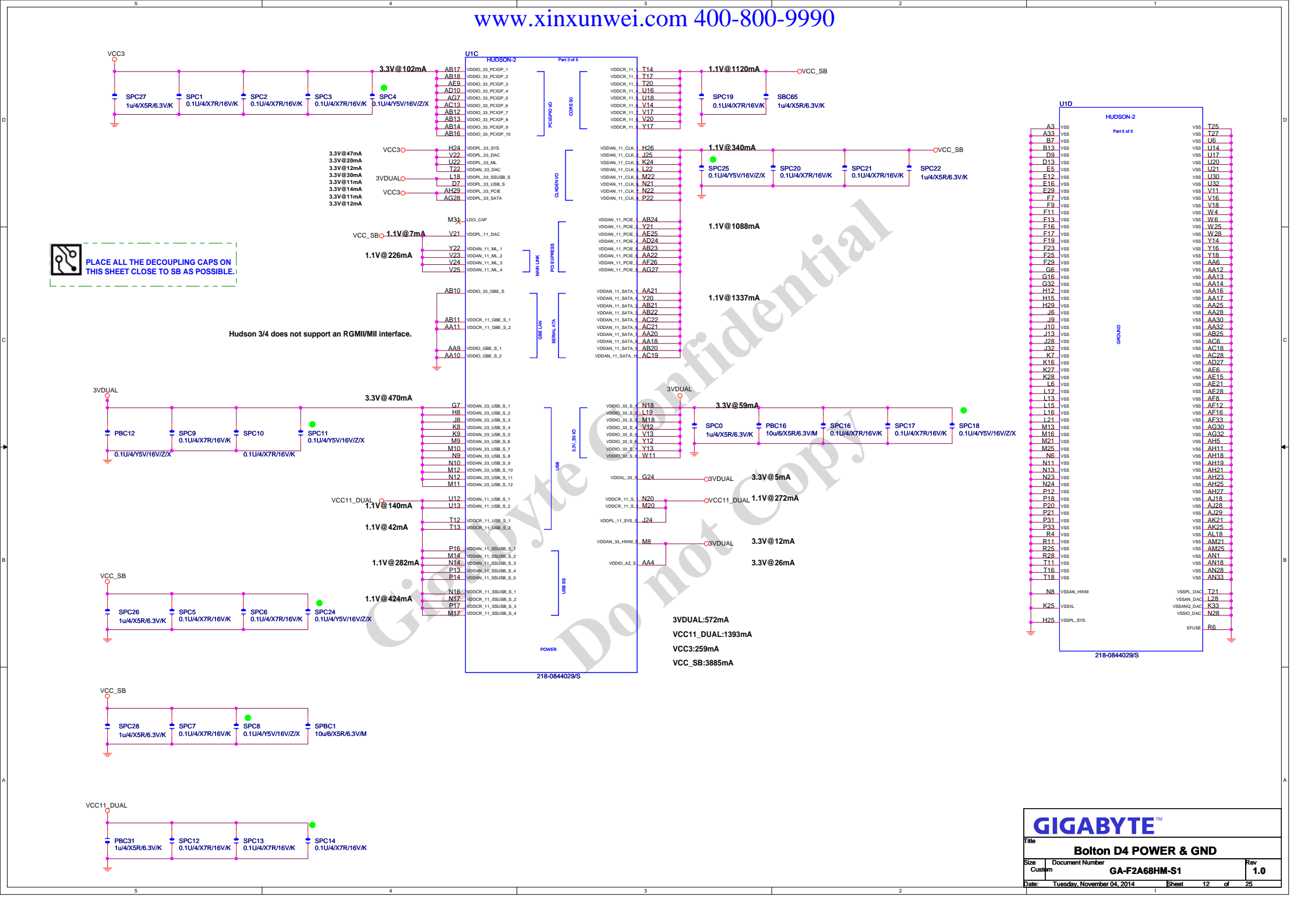
PC42 MASK/C0402-SHORT-45/X

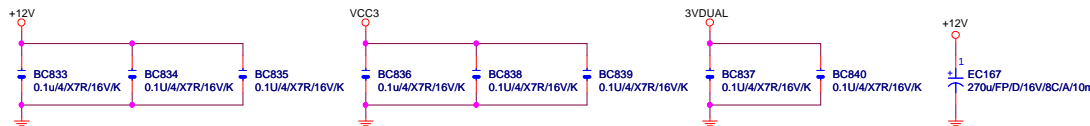
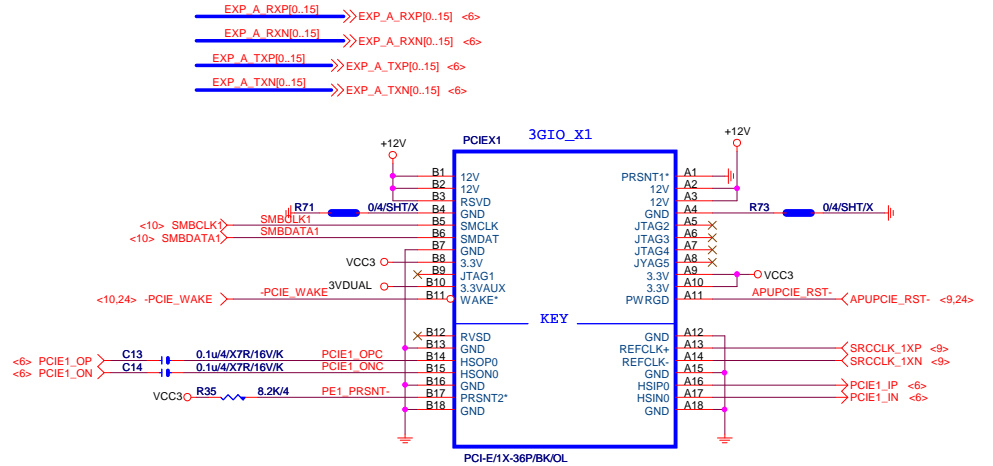
PC43 MASK/C0402-SHORT-45/X

PC44 MASK/C0402-SHORT-45/X

PC45 MASK/C0402-SHORT-45/X

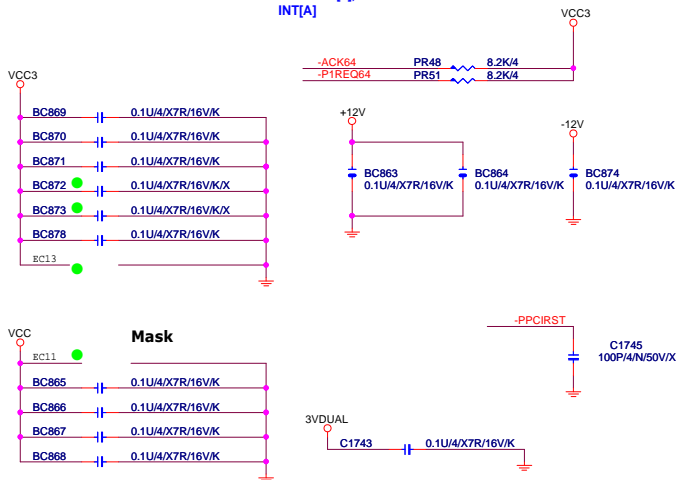
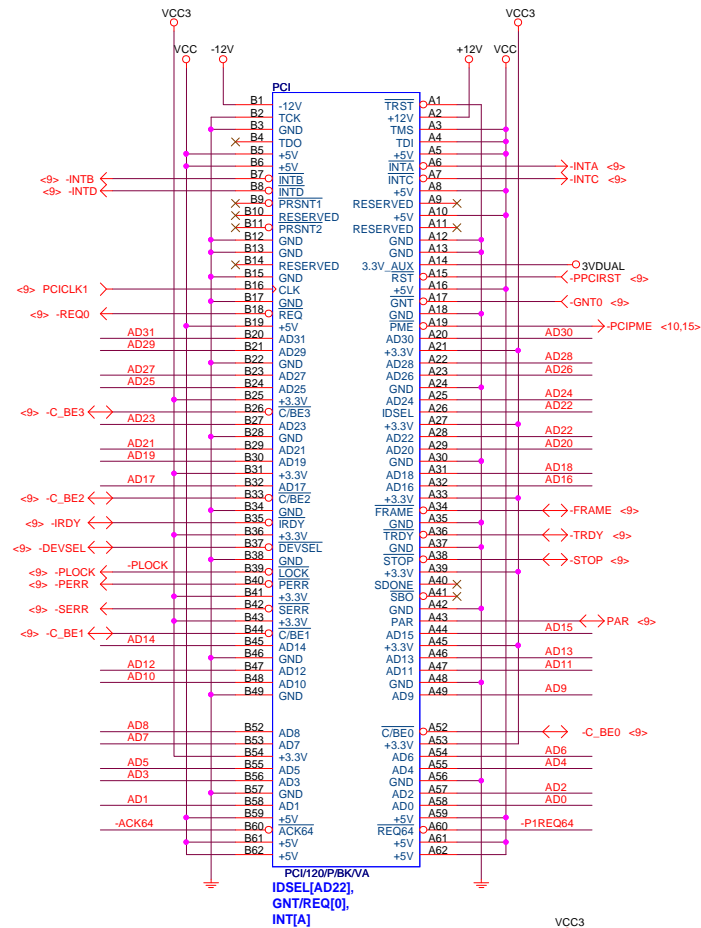




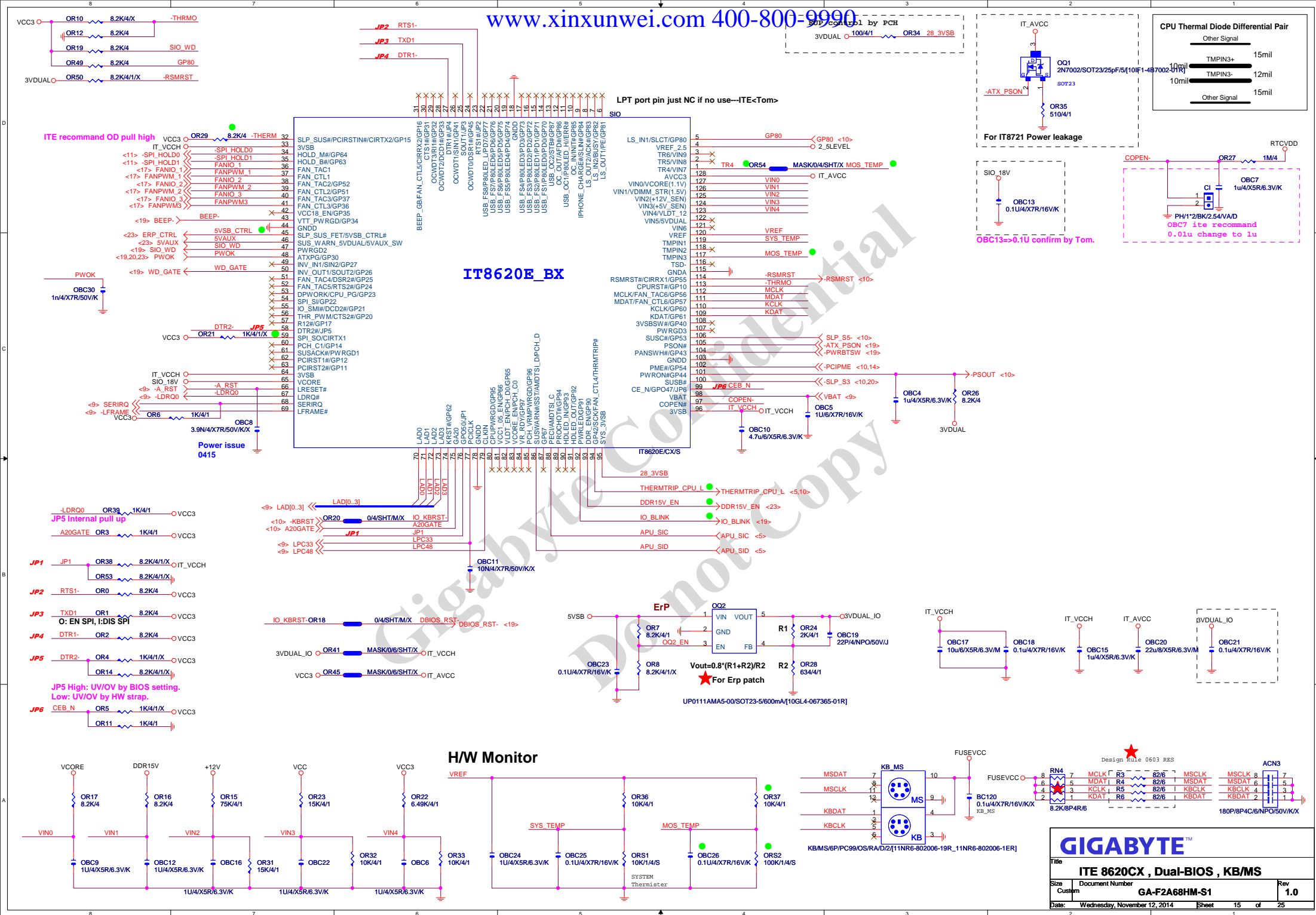


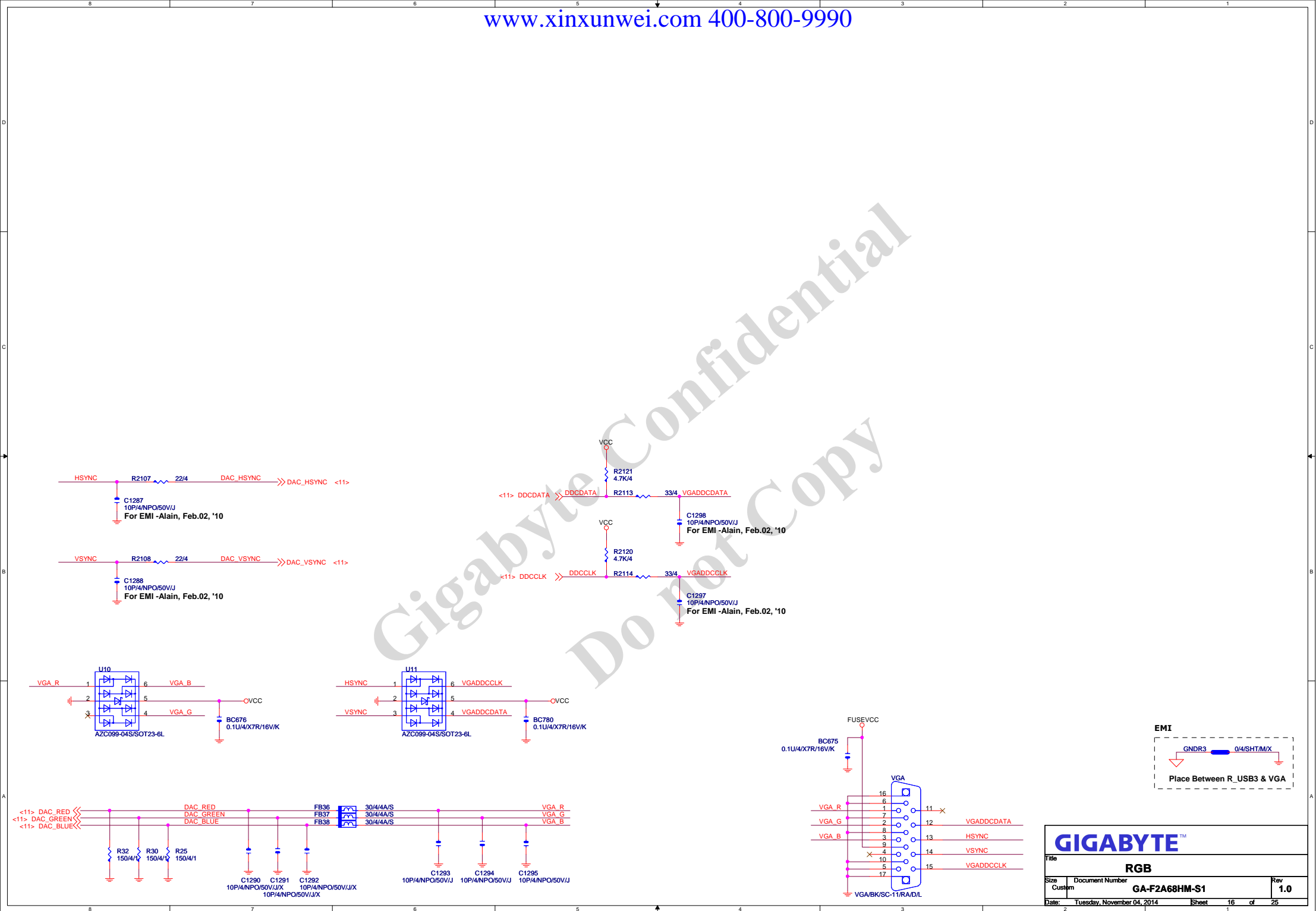
PCI SLOT 1,2

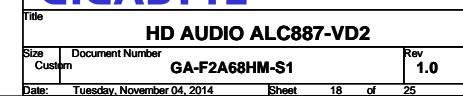
<9> AD[0..31] <-> AD[0..31]

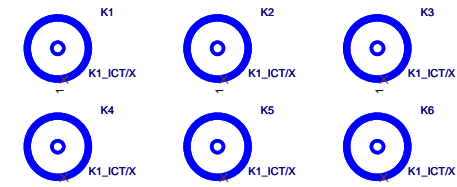
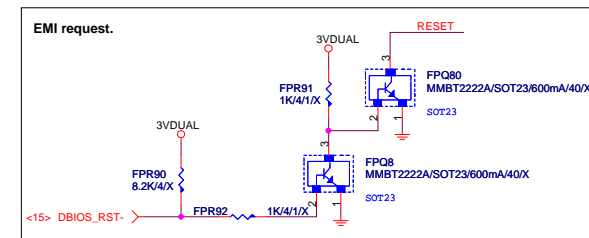
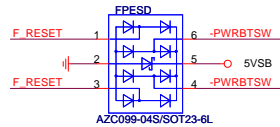
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PCI SLOT		
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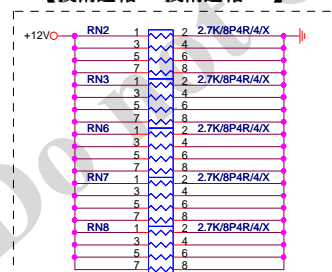




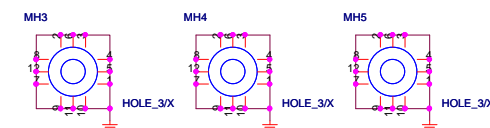
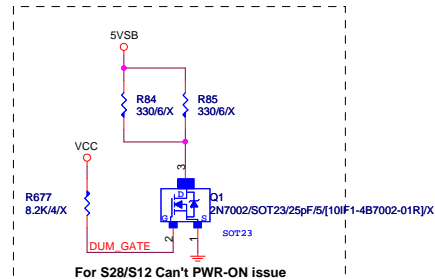


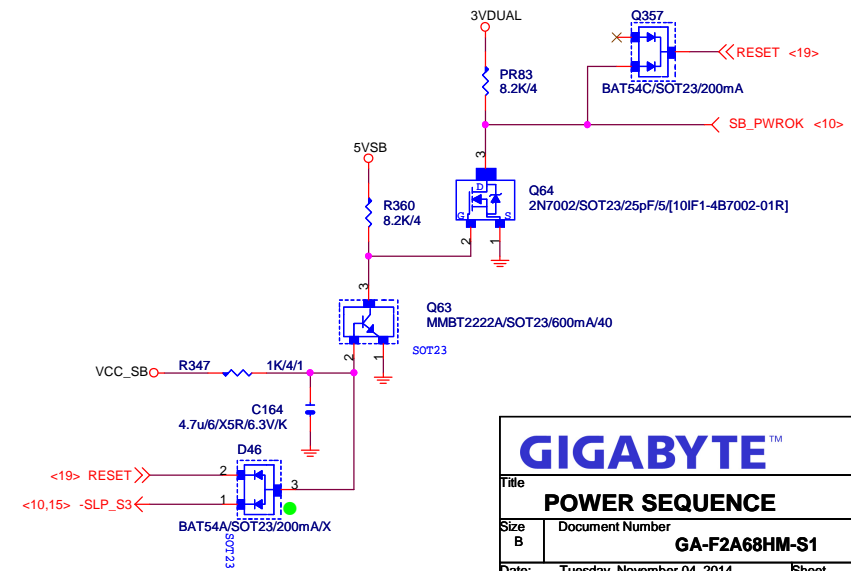
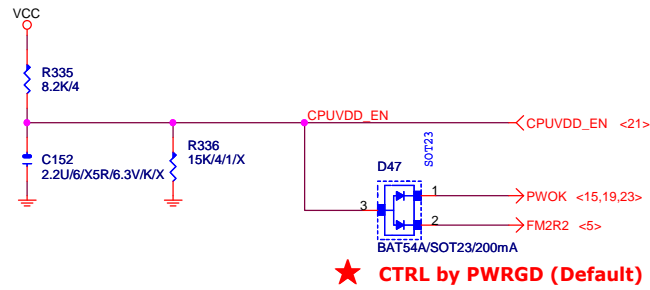
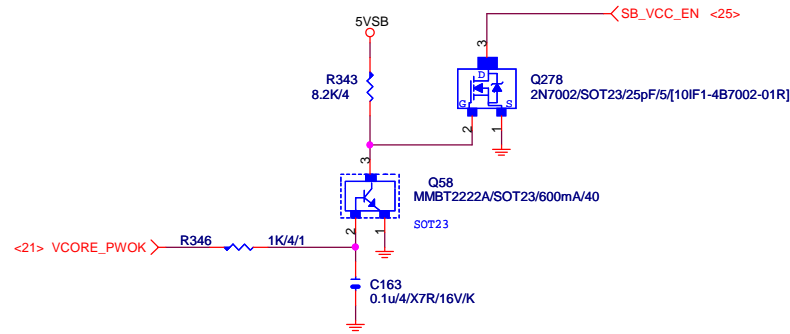
The figure shows three circuit diagrams, labeled MH1, MH2, and MH8, each representing a different model of a component. Each diagram features a circular component with six pins: 1, 2, 4, 5, 8, and 12. The connections are as follows:

- MH1:** Pin 1 is connected to ground. Pin 2 is connected to pin 4. Pin 4 is connected to pin 5. Pin 5 is connected to pin 8. Pin 8 is connected to pin 12. Pin 12 is connected to HOLE_3X.
- MH2:** Pin 1 is connected to ground. Pin 2 is connected to pin 4. Pin 4 is connected to pin 5. Pin 5 is connected to pin 8. Pin 8 is connected to pin 12. Pin 12 is connected to HOLE_3X.
- MH8:** Pin 1 is connected to ground. Pin 2 is connected to pin 4. Pin 4 is connected to pin 5. Pin 5 is connected to pin 8. Pin 8 is connected to pin 12. Pin 12 is connected to HOLE_30.



To fix 12V light load abnormal issue

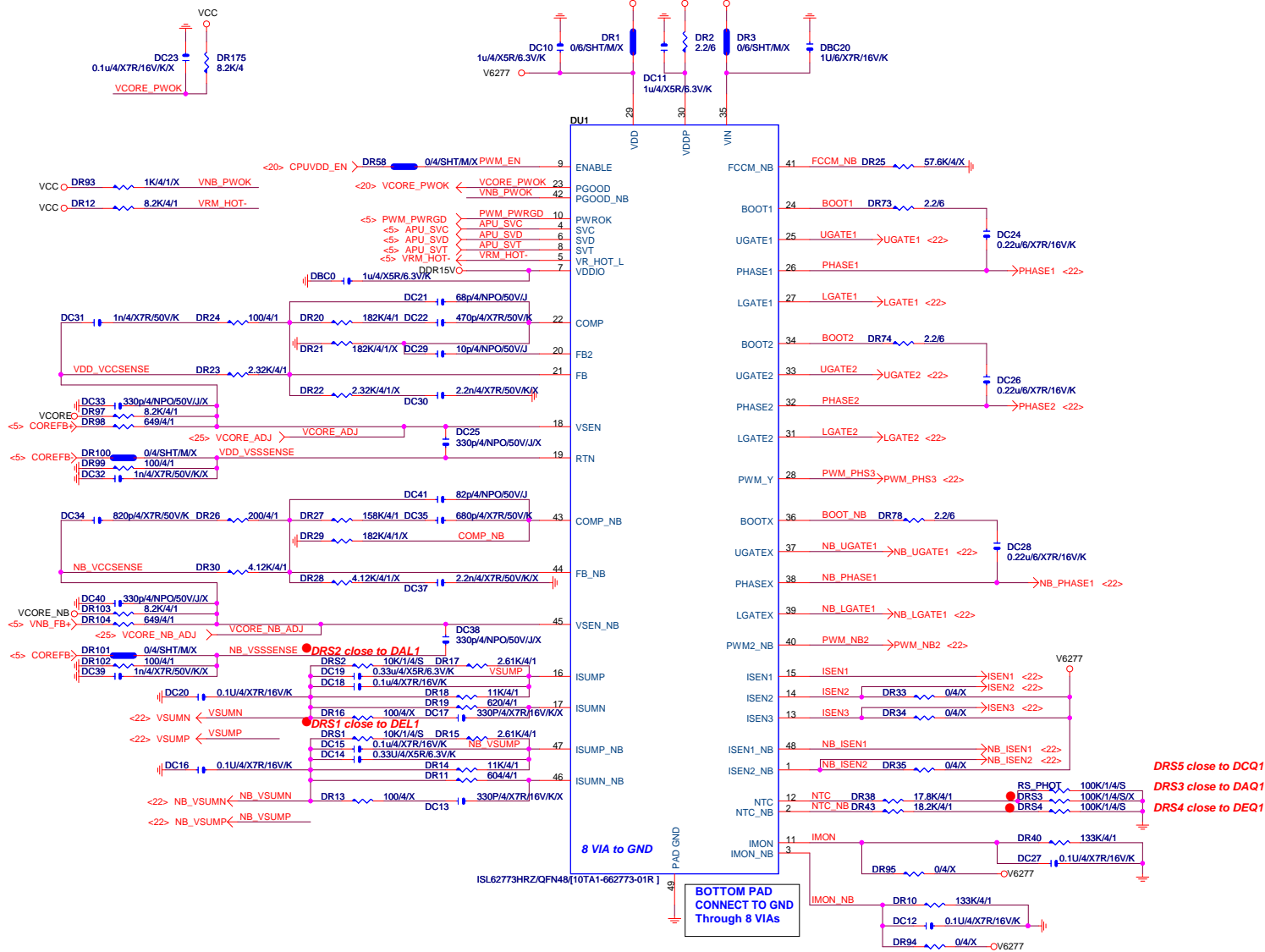


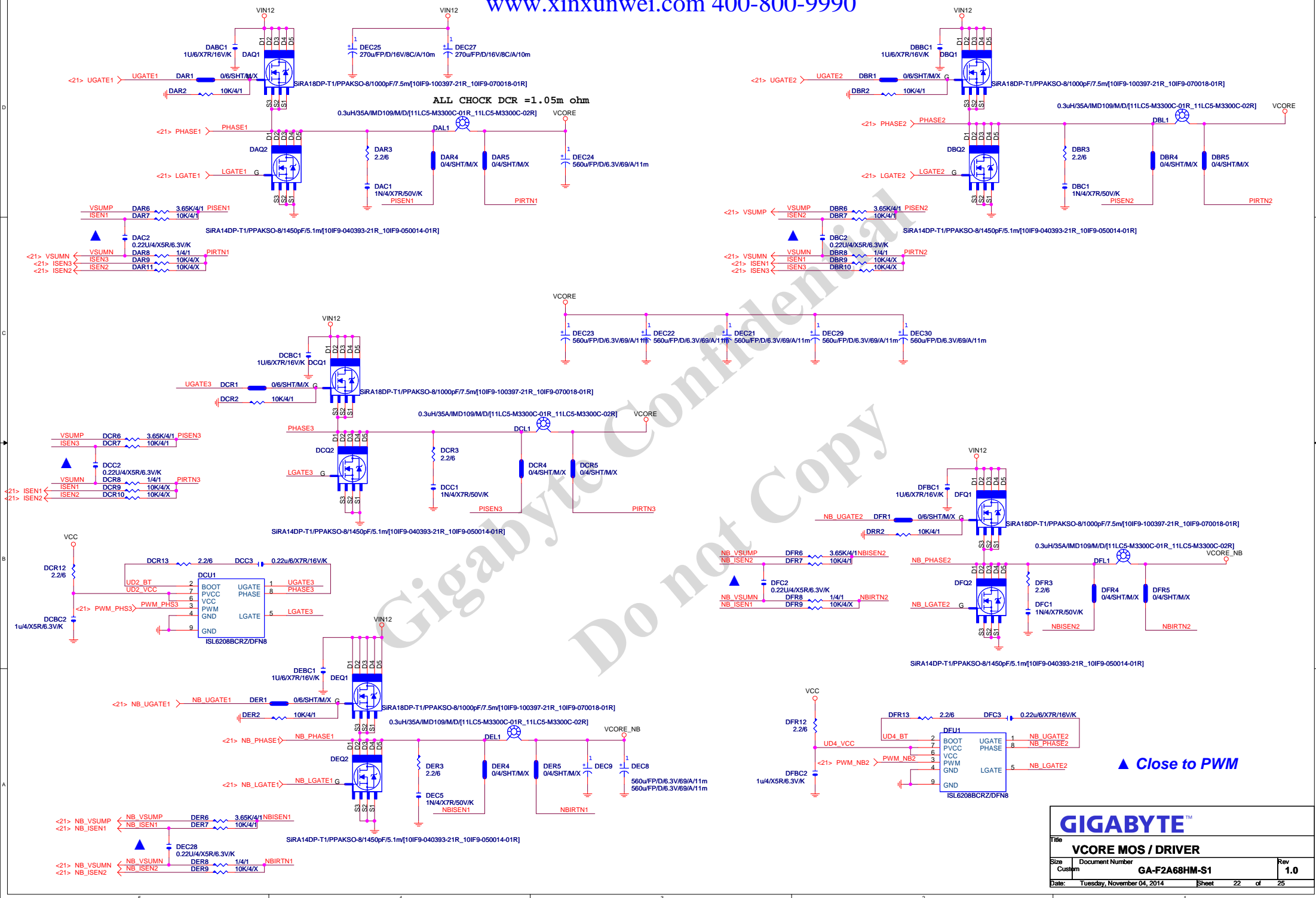


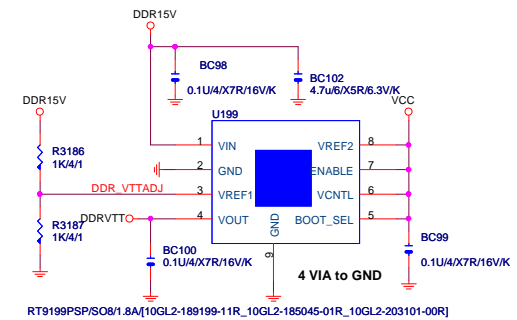
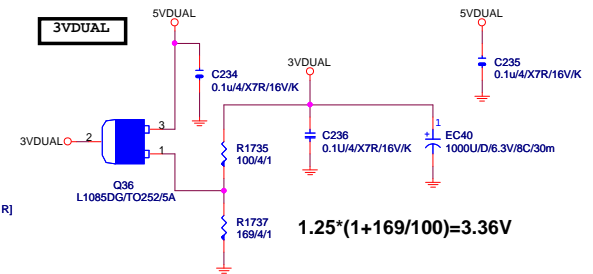
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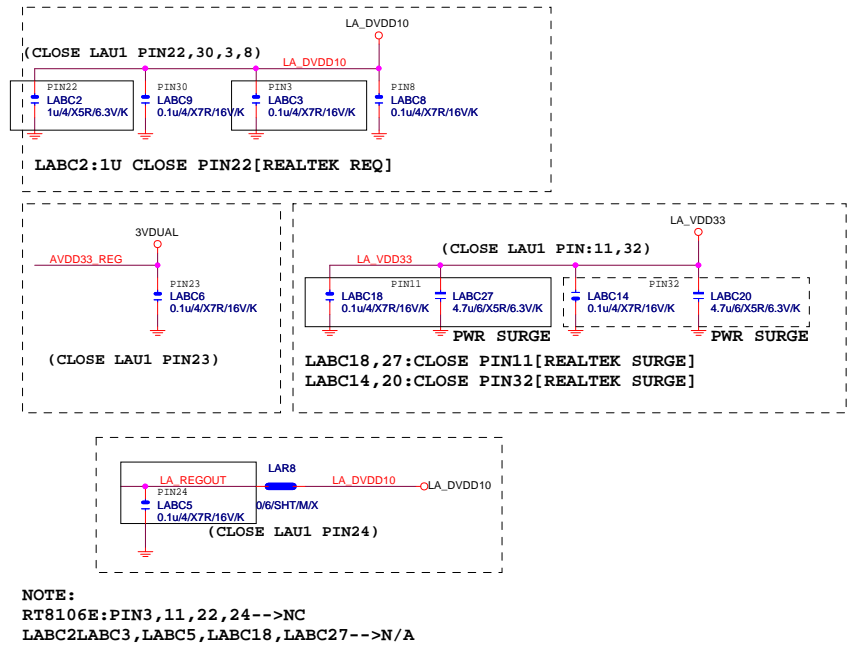
POWER SEQUENCE

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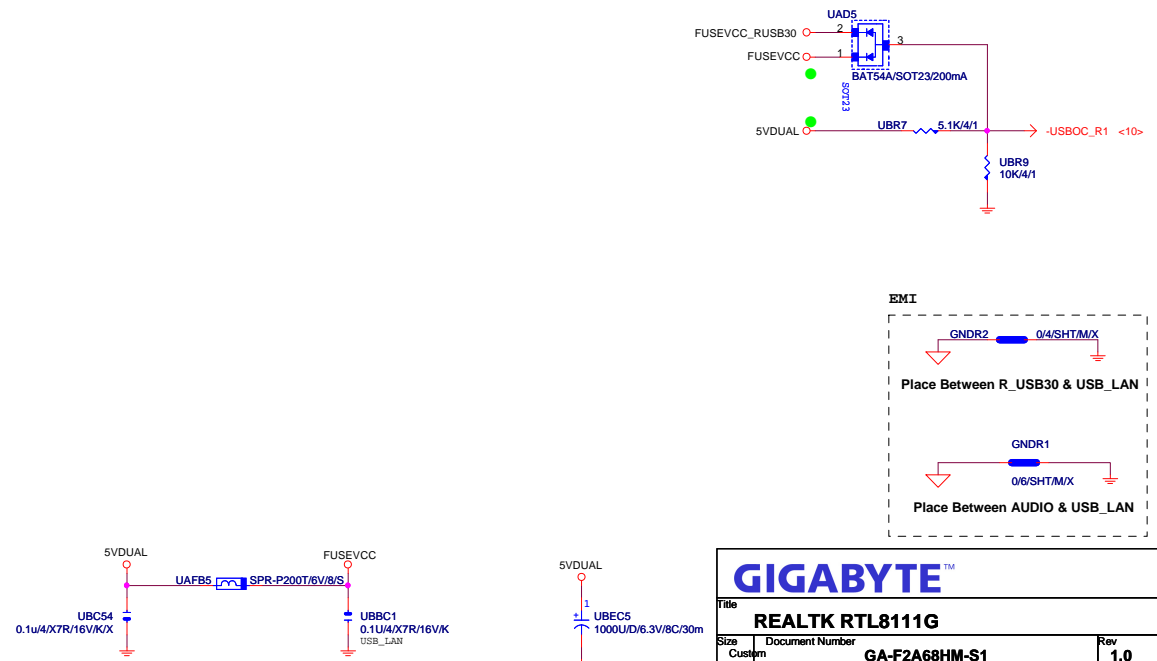




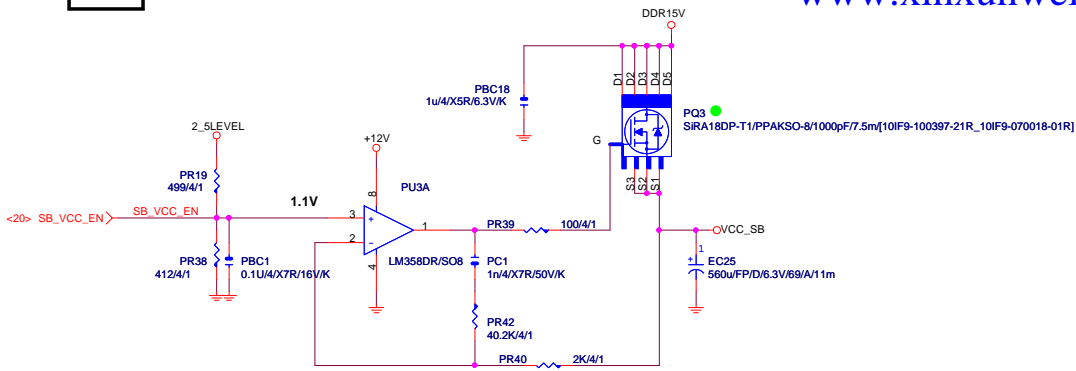




USB_LAN CONNECTOR

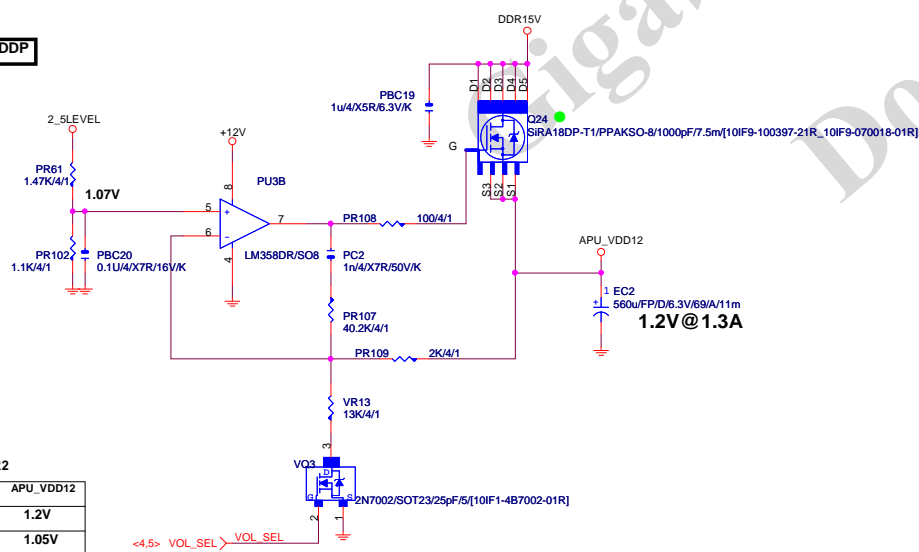


VCC_SB



2_SLEVEL
BC0
22u/8/X5R/6.3V/M
Near PR19 / PR61

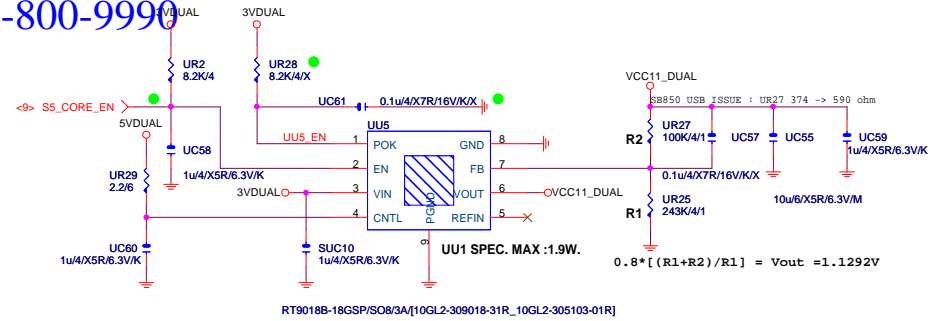
APU_VDDP



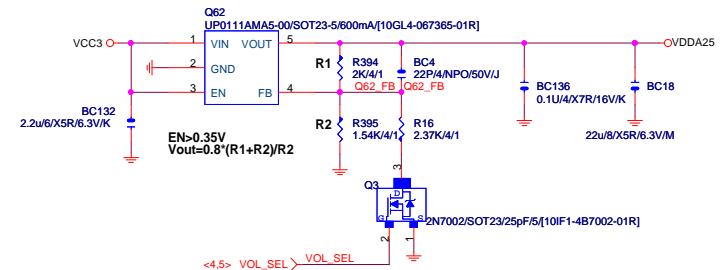
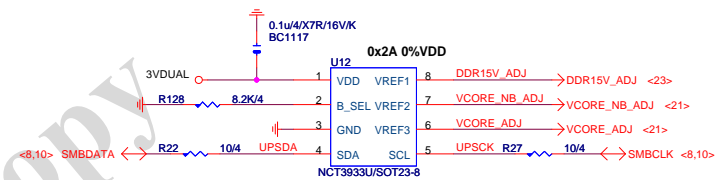
$$V_{out} = 1.07 \cdot (R1 + R2) / R2$$

APU	VOL_SEL	APU_VDD12
FM2	1	1.2V
FM2+	0	1.05V

<4,5> VOL_SEL > VOL_SEL



【技術通報R&D技術通報156】
RT9018 (RICHTEK) 與 NCT3730 (NUVOTON),
EM5103GE (EMC) 做共用, 針對 PIN7 (FB) 分壓阻值部份
(R1/R2) 須做修改為 100K 以上電阻值



APU	VOL_SEL	VDDA25
FM2	1	2.5V
FM2+	0	1.8V

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